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EXAMINER	
LEE, SHUN K	

ART UNIT	PAPER NUMBER
2884	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,480	CHOO ET AL.	
	Examiner	Art Unit	
	Shun Lee	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20050923*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

National Stage Application

Claim Objections

1. Claims 1, 11, 12, and 15 are objected to because of the following informalities:

(a) in claim 1, "to" on line 6 should probably be --from--;

(b) in claim 11, "corresponding to the first and second conductive lines, thereby exposing" on lines 10-11 should probably be --to expose-- (since the drain electrode does not correspond to the second conductive line Vcom in Fig. 2);

(c) in claim 12, "transparent layer" on line 3 should probably be --transparent electrode--; and

(d) in claim 15, "the second transparent electrode includes a plurality of stages sequentially making an electrical contact with each other, each of the stages including a plurality of thin film transistors comprising amorphous silicon, and" on line 1 should probably be --the second switching element is a plurality of thin film transistors comprising amorphous silicon, said plurality of thin film transistors arranged in a plurality of stages sequentially making an electrical contact with each other, and each stage--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kameshima (US 2002/0196898).

In regard to claim **1**, Kameshima discloses (Figs. 7 and 8) an array panel comprising:

(a) an array portion formed on a first region of a substrate, the array portion (described in paragraphs 46 and 47 as comprising TFTs and storage capacitors for) accumulating and storing electrons generated in accordance with light supplied from outside; and

(b) a gate-driving portion (22) formed on a second region of the substrate, the gate driving portion (22) applying a scanning signal for extracting the electrons to the array portion.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kameshima (US 2002/0196898) in view of Jeon *et al.* (US 2002/0149318).

In regard to claims **2** and **3** which are dependent on claim 1, the panel of Kameshima lacks that the gate-driving portion includes a plurality of stages sequentially making an electrical contact with each other, each of the stages including a plurality of thin film transistors comprising amorphous silicon, and including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register, and wherein each of the stages includes: a pull-up portion that provides a corresponding signal to the output terminal among a first clock signal and a second clock signal, the second clock signal having a phase opposite to the phase of the first clock signal; a pull-down portion that applies a first voltage to the output terminal; a pull-up driver connected to an input node of the pull-up portion, the pull-up driver being turned on in accordance with the output signal of a previous stage, and being turned off in accordance with a first control signal so that the first clock signal or a second control signal is removed to remove the second clock signal; and a pull-down driver connected to an input node of the pull-down portion, the pull-down driver being turned off in accordance with an input signal, and being turned on in accordance with the first control signal or the second control signal, wherein, the first clock signal

and the first control signal are transmitted to odd numbered stages, and the second clock signal and the second control signal are transmitted to even numbered stages. However, Kameshima also disclose (paragraph 47) that the gate driver (22 in Fig. 8) comprise of a shift register (not shown in Fig. 8). Since Kameshima does not disclose and/or require a specific shift register, one having ordinary skill in the art at the time of the invention would reasonably interpret the unspecified shift register of Kameshima as any one of the known conventional shift registers that did not require a detailed description. Further, Jeon *et al.* teach a shift register (164 in Fig. 5) comprising a plurality of stages sequentially making an electrical contact with each other, each of the stages including an input terminal, an output terminal (through which corresponding signals are transmitted), and a plurality of thin film transistors comprising amorphous silicon (paragraph 243) with a first clock signal and first control signal transmitted to odd numbered stages and second clock signal and second control signal transmitted to even numbered stages (paragraphs 109 and 110), a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, and wherein each of the stages includes: a pull-up driver (194 in Fig. 16) connected to an input node of a pull-up portion (190 in Fig. 16) that provides a corresponding signal to the output terminal among a first clock signal and a second clock signal having a phase opposite (paragraph 109) to the phase of the first clock signal; a pull-down driver (196 in Fig. 16) connected to an input node of a pull-down portion (192 in Fig. 16) that applies a first voltage to the output terminal; the pull-up driver being turned on in accordance with the output signal of a previous stage, and

being turned off in accordance with a first control signal so that the first clock signal or a second control signal is removed to remove the second clock signal; and the pull-down driver being turned off in accordance with an input signal, and being turned on in accordance with the first control signal or the second control signal. Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to provide a known conventional shift register (*e.g.*, comprising a plurality of stages, each including a pull-up driver connected to an input node of a pull-up portion and a pull-down driver connected to an input node of a pull-down portion) as the unspecified shift register in the panel of Kameshima.

7. Claims 4, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* (US 2001/0049154) in view of Kameshima (US 2002/0196898).

In regard to claims **4**, **6**, and **8**, Choo *et al.* disclose (Figs. 1-5) disclose an array panel comprising:

(a) a substrate (1, 171);

(b) a gate line (50, 150) extended on the substrate (1, 171) in a first direction;

(c) a data line (53, 153) extended on the substrate (1, 171) in a second direction;

(d) a switching element (T) including a gate electrode (73, 173), a source electrode (32, 132), and a drain electrode (33, 133), the switching element (T) being formed in a pixel region defined by the gate (50, 150) and the data (53, 153) lines;

(e) a photoelectric cell (2) for generating electrons in proportion with the intensity of light supplied from outside, thereby generating an electrical signal;

(f) a pixel electrode (62, 211) formed in the pixel region, the pixel electrode (62, 211) comprises indium tin oxide ("ITO"; paragraphs 20 and 53) and gathering electrons generated from the photoelectric cell (2);

(g) an organic layer (83, 183; paragraphs 17 and 51) interposed between the pixel electrode (62, 211) and the switching element (T);

(h) a storage capacitor (S) formed in the pixel region, the storage capacitor (S) storing the electrons gathered by the pixel electrode (62, 211);

(i) a gate driver (*i.e.*, not shown "scanning integrated circuit"; paragraph 8) making an electrical contact with the gate line on the substrate (1, 171), the gate driver sequentially providing a scan signal for driving the switching element (T); and

(j) a data pad (paragraph 21) making an electrical contact with an end portion of the data line on the substrate (1, 171), the electrons stored in the storage capacitor (S) being extracted to the data pad through the switching element (T) in case that the switching element (T) is turned on.

The panel of Choo *et al.* lacks that the data pad makes an electrical contact with an end portion of the data line and the gate driver makes an electrical contact with an end portion of the gate line. Since Choo *et al.* do not disclose and/or require a specific scanning and/or data processing integrated circuitry location, one having ordinary skill in the art at the time of the invention would reasonably interpret the unspecified circuitry location of Choo *et al.* as any one of the known conventional circuitry locations that did not require a detailed description. Further, Kameshima teaches (Figs. 7 and 8) that scanning and/or data processing integrated circuitry are located at the ends of the gate

and data lines. Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to locate the data pad and the gate driver at a known conventional location (*e.g.*, at the ends of the data and gate lines, respectively) in the panel of Kameshima.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* in view of Kameshima as applied to claim 4 above, and further in view of Jeon *et al.* (US 2002/0149318).

In regard to claim **5** which is dependent on claim 4, the modified panel of Choo *et al.* lacks that the gate driver includes a plurality of stages sequentially making an electrical contact with each other, each stage including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register. However, Choo *et al.* also disclose (paragraph 8) that the TFT "T" is turned ON by the scanning integrated circuit (not shown). Since Choo *et al.* do not disclose and/or require a specific scanning integrated circuit, one having ordinary skill in the art at the time of the invention would reasonably interpret the unspecified scanning circuit of Choo *et al.* as any one of the known conventional scanning circuits that did not require a detailed description. Further, Jeon *et al.* teach a scanning circuit including shift register (164 in Fig. 5) comprising a plurality of stages sequentially making an electrical contact with each other, each of the stages including an input terminal, an output terminal (through which corresponding signals are transmitted), and

a plurality of thin film transistors comprising amorphous silicon (paragraph 243) with a first clock signal and first control signal transmitted to odd numbered stages and second clock signal and second control signal transmitted to even numbered stages (paragraphs 109 and 110), a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, and wherein each of the stages includes: a pull-up driver (194 in Fig. 16) connected to an input node of a pull-up portion (190 in Fig. 16) that provides a corresponding signal to the output terminal among a first clock signal and a second clock signal having a phase opposite (paragraph 109) to the phase of the first clock signal; a pull-down driver (196 in Fig. 16) connected to an input node of a pull-down portion (192 in Fig. 16) that applies a first voltage to the output terminal; the pull-up driver being turned on in accordance with the output signal of a previous stage, and being turned off in accordance with a first control signal so that the first clock signal or a second control signal is removed to remove the second clock signal; and the pull-down driver being turned off in accordance with an input signal, and being turned on in accordance with the first control signal or the second control signal. Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to provide a known conventional scanning circuit (*e.g.*, comprising a plurality of stages, each including a pull-up driver connected to an input node of a pull-up portion and a pull-down driver connected to an input node of a pull-down portion) as the unspecified scanning circuit in the modified panel of Choo *et al.*

9. Claims 7, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* in view of Kameshima as applied to claim 4 above, and further in view of Jeromin *et al.* (US 6,075,248).

In regard to claim **7**, **9**, and **10** which are dependent on claim 4, the modified panel of Choo *et al.* lacks that the pixel electrode is disposed on a whole surface of the switching element and the gate driver with an organic layer interposed between the pixel electrode and the gate driver. However, Jeromin *et al.* teach (column 4, lines 21-24) to extend the electrode (18 in Fig. 1) over the FET (22 in Fig. 1). Further, Jeromin *et al.* teach to provide shielding electrodes (*e.g.*, 256 in Fig. 7) for circuitry, in order to minimize noise (column 4, line 64 to column 5, line 13). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to dispose the second transparent electrode on an insulating organic layer covering a whole surface of the first and second switching element in the modified panel of Choo *et al.*, in order to minimize noise.

10. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* (US 2001/0049154) in view of Fender *et al.* (US 5,300,784).

In regard to claims **11** and **12**, Choo *et al.* disclose (Figs. 1-5) a method of manufacturing an array panel, the method comprising:

(a) forming first (T) and second (*i.e.*, not shown "scanning integrated circuit"; paragraph 8) switching elements, a first conductive line (53, 153) for a data pad (paragraph 21) and a second conductive line (42, 142) for a storage capacitor (S), the first switching element (T) corresponding to a pixel region of a substrate (1, 171);

(b) forming a first transparent electrode (58, 158) on the second (42, 142) conductive line;

(c) sequentially coating an insulating (*i.e.*, "Silicon Nitride"; paragraphs 16 and 50) layer (81, 181) and an organic layer (83, 183; paragraphs 17 and 51) on the first transparent electrode (58, 158);

(d) partially removing the organic layer (83, 183) corresponding to the second (42, 142) conductive line and a drain electrode (33, 133) of the first switching element (T);

(e) partially removing the insulating layer (81, 181) to expose drain electrode (33, 133) of the first switching element (T);

(f) forming a second transparent electrode (62, 211) for collecting electrons, the second transparent electrode (62, 211) being electrically connected to the drain electrode (33, 133);

(g) forming a light conductive semiconductor layer (2); and

(h) forming an electrode (7) on the light conductive semiconductor layer (2).

The method of Choo *et al.* lacks an explicit description of forming a protecting layer on the exposed organic layer and the second transparent layer and that the data pad is obtained by partially removing the organic layer and the insulating layer and forming the second transparent electrode to electrically connect to the exposed first transparent electrode corresponding to the first conductive line. However, Fender *et al.* teach (column 7, lines 1-20) to provide an interface layer (13 in Fig. 2) adjacent an armphorphous selenium photoreceptor layer (1 in Fig. 2) in order to protect against

crystallite formation. Further, Choo *et al.* also disclose partially removing the organic layer and the insulating layer in order to expose the conductive lines so as to form electrical connections. Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to form a protecting layer on the exposed organic layer and the second transparent layer in the method of Choo *et al.*, in order to protect against crystallite formation. Further, it would have been obvious to one having ordinary skill in the art at the time of the invention to partially removing the organic layer and the insulating layer in the method of Choo *et al.*, in order to expose the data pad so as to allow the formation of electrical connections to data processing circuitry.

11. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* in view of Fender *et al.* as applied to claim 11 above, and further in view of Jeromin *et al.* (US 6,075,248).

In regard to claims **13** and **14** which are dependent on claim 11, the modified method of Choo *et al.* lacks that the second transparent electrode is disposed on a whole surface of the first and second switching element. However, Jeromin *et al.* teach (column 4, lines 21-24) to extend the electrode (18 in Fig. 1) over the FET (22 in Fig. 1). Further, Jeromin *et al.* teach to provide shielding electrodes (*e.g.*, 256 in Fig. 7) for circuitry, in order to minimize noise (column 4, line 64 to column 5, line 13). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to dispose the second transparent electrode on a whole surface of the first and second switching element in the modified method of Choo *et al.*, in order to minimize noise.

12. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choo *et al.* in view of Fender *et al.* as applied to claim 11 above, and further in view of Jeon *et al.* (US 2002/0149318).

In regard to claim **15** which is dependent on claim 11, the modified method of Choo *et al.* lacks an explicit description that the second transparent electrode includes a plurality of stages sequentially making an electrical contact with each other, each of the stages including a plurality of thin film transistors comprising amorphous silicon, and including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register. However, Choo *et al.* also disclose (paragraph 8) that the TFT "T" is turned ON by the scanning integrated circuit (not shown). Since Choo *et al.* do not disclose and/or require a specific scanning integrated circuit, one having ordinary skill in the art at the time of the invention would reasonably interpret the unspecified scanning circuit of Choo *et al.* as any one of the known conventional scanning circuits that did not require a detailed description. Further, Jeon *et al.* teach a scanning circuit including shift register (164 in Fig. 5) comprising a plurality of stages sequentially making an electrical contact with each other, each of the stages including an input terminal, an output terminal (through which corresponding signals are transmitted), and a plurality of thin film transistors comprising amorphous silicon (paragraph 243) with a first clock signal and first control signal transmitted to odd numbered stages and second clock signal and second control signal transmitted to

even numbered stages (paragraphs 109 and 110), a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, and wherein each of the stages includes: a pull-up driver (194 in Fig. 16) connected to an input node of a pull-up portion (190 in Fig. 16) that provides a corresponding signal to the output terminal among a first clock signal and a second clock signal having a phase opposite (paragraph 109) to the phase of the first clock signal; a pull-down driver (196 in Fig. 16) connected to an input node of a pull-down portion (192 in Fig. 16) that applies a first voltage to the output terminal; the pull-up driver being turned on in accordance with the output signal of a previous stage, and being turned off in accordance with a first control signal so that the first clock signal or a second control signal is removed to remove the second clock signal; and the pull-down driver being turned off in accordance with an input signal, and being turned on in accordance with the first control signal or the second control signal. Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to provide a known conventional scanning circuit (*e.g.*, comprising a plurality of stages, each including a pull-up driver connected to an input node of a pull-up portion and a pull-down driver connected to an input node of a pull-down portion) as the unspecified scanning circuit in the modified method of Choo *et al.*

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shun Lee whose telephone number is (571) 272-2439. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. L./
Examiner, Art Unit 2884

/Constantine Hannaher/
Primary Examiner, Art Unit 2884